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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,614	10/02/2003	Srinivasan Chakravarthi	TI--33161.2	8936

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/677,614	**Applicant(s)** CHAKRAVARTHI ET AL.	
	Examiner Jennifer M. Dolan	**Art Unit** 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/2/03*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. The Examiner notes that claims 1-16 were canceled from the application in the preliminary amendment of 10/2/03. Claims 17-21, grouped as a single invention (Group III) in the restriction requirement of 1/22/05, are the only pending claims. Hence, the restriction requirement is withdrawn and considered moot.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 17-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,812,523 to Chu et al. in view of U.S. Patent No. 5,976,939 to Thompson et al. and U.S. Patent No. 6,069,062 to Downey

Regarding claims 17 and 21, Chu discloses a method of forming a shallow junction for a CMOS device (see columns 1-2), comprising: pre-amorphizing a first layer of the semiconductor crystal adjacent the surface (column 4, lines 48-67, column 7, lines 13-16; see figure 9A); heating to regrow the semiconductor crystal (any of the subsequent heat treatments, such as the dopant diffusion anneal, will re-crystallize the silicon layer; see column 4, lines 60-67; column 5, line 48; column 7, lines 20-24; alternatively, see column 6, lines 20-30; low temperature anneal), forming a target dopant layer comprising a target dopant over the surface (column 5, lines 5-7; column 5, lines 45-55); and annealing to cause the target dopant to diffuse from the target dopant layer into the surface (column 8, lines 60-67). It is apparent that Chu is drawn to a CMOS structure (see columns 1-2) and forming narrow dopant junctions therein. Thus, a person skilled in the art could reasonably deduce that Chu must include the claimed gate formation and patterning steps in order to attain the CMOS structure.

Chu, however, fails to expressly disclose the MOSFET forming steps, including forming the gate layer, forming the poly layer, and patterning such layers through photolithography. Chu further fails to disclose implanting a portion within the first layer with a temporary impurity atom.

Thompson discloses the application of a narrow junction structure to a MOSFET formation process, wherein a gate layer is formed (column 3, lines 10-13), a poly layer is formed on the gate layer (column 3, lines 13-15), standard photolithography, which is understood to inherently include photoresist deposition and patterning, is performed (see column 3, lines 14-16), and etching is performed to pattern the gate and poly layers, thus exposing the substrate (column 3, lines 14-16; figure 1).

Downey discloses that boron diffusion junctions are made even shallower by implanting a temporary impurity atom, such as fluorine, into amorphous regions of a substrate before boron diffusion (column 2, lines 50-67; column 4, line 29 – column 5, line 30; table 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the CMOS formation method of Chu include the gate formation steps taught by Thompson, and to modify the method to further include the temporary impurity atom implant suggested by Downey. The rationale is as follows: A person having ordinary skill in the art would have been motivated to specify formation of the gate layers including patterning by standard photolithography, because Chu explicitly states that the method therein is drawn to a CMOS, which is well understood in the art as including patterned gate and gate oxide layers. Thus, the inclusion of the specific gate formation steps as in Thompson would be an extremely trivial and apparent modification to the CMOS formation method in Chu. A person skilled in the art would further have been motivated to implant fluorine atoms within the amorphous Si region, because Downey shows that fluorine implants further impede the diffusion of boron through the wafer, thus causing formation of very shallow junctions (see Downey, column 2, liens 50-67; column 4, line 29 – column 5, line 30). It is reasonably expected that the fluorine implant in Downey and the boron diffusion from a solid source in Chu would have some sort of cumulative effect when combined, since Chu shows that boron diffused from a layer directly on the surface, rather than a layer within the surface, has greater difficulty in diffusing into regions with high interstitial densities (see Chu, column 5, lines 1-35), and thus has less tendency to spread deeply into the wafer, whereas the fluorine implant causes fluorine atoms to actively occupy and getter interstitial sites, which further prevents boron diffusion (see Downey, column 4, lines 29-67).

Regarding claims 18 and 19, Chu as modified by Thompson and Downey, discloses a MOSFET structure, but Chu fails to explicitly disclose the geometric disposition of the target boron dopant layer.

Thompson teaches that for forming a shallow junction MOSFET device, the target dopant layer (16) is disposed as a spacer layer over the gate structure (figures 1-4), with additional spacer layers (30, 31) disposed thereon, wherein the spacer layers are etched (figure 4) prior to the step of dopant diffusion from the target layer (figure 6 – formation of regions 40-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the combination of Chu, Thompson, and Downey as applied to claim 17, supra, such that the target dopant layer is disposed as a spacer layer, as further suggested by Thompson. The rationale is as follows: A person having ordinary skill in the art would have been motivated to dispose the target dopant layer as a spacer layer, because doing so allows for the formation of shallow junction regions that are precisely controlled in extent as well as self-aligned to the gate structure (see Thompson, column 4, lines 1-10, 45-57).

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chu in view of Thompson and Downey as applied to claim 17 above, and further in view of U.S. Patent Publication No. 2001/0041432 to Lee.

Chu as modified by Thompson and Downey teaches silicon oxide gate layers, and not high-k gate layers.

Lee teaches that for shallow junction MOSFETs, any of silicon dioxide, silicon nitride (reasonably considered high-k), or various metal oxides (aluminum oxide and titanium oxide are reasonably considered to be high-k) are well known and appropriately used as gate layers (see paragraph 0040).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Chu as modified by Thompson and Downey, such that the gate layer is formed from high-k dielectrics, as suggested by Lee. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a high-k gate oxide layer, because Lee shows that both silicon oxide and various high-k materials are equally well known and compatible with standard shallow-junction MOSFET formation, and thus, any of these materials could reasonably be substituted for the SiO in Chu as modified by Thompson and Downey. A person skilled in the art would find it advantageous to select a high-k gate oxide, since such a material can be provided in a thicker layer than silicon oxide having the same general electrical properties, thus improving ease of fabrication, controllability of the thickness, and hence, the electrical properties, and improved resistance to dielectric breakdown, as is well known and appreciated by a person having ordinary skill in the art.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,153,920 to Gossman discloses carbon implantation to control diffusion of dopants.

b. U.S. Patent No. 5,994,175 to Gardner et al. discloses a combination of fluorine implants, boron implants, and silicon implants in order to reduce boron diffusion.

c. Appl. Phys. Lett. article to Saito discloses the use of fluorine as both a pre-amorphizing implant and a temporary impurity implant in order to reduce boron channeling.

d. Appl. Phys. Lett article to Huang et al. discloses a combination of a low energy B implant, preamorphization of the substrate, and fluorine implanting to control B diffusion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Carl Whitehead
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